

Fig. 1 (prior art)

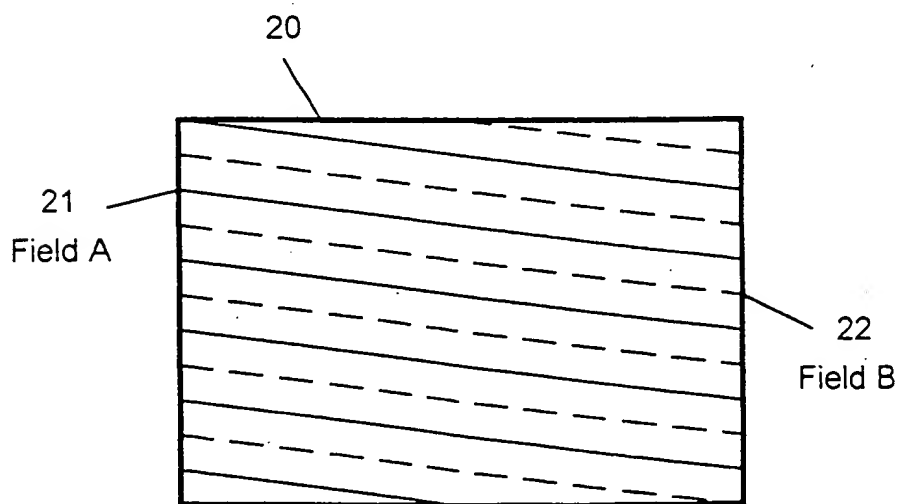


Fig. 2 (prior art)

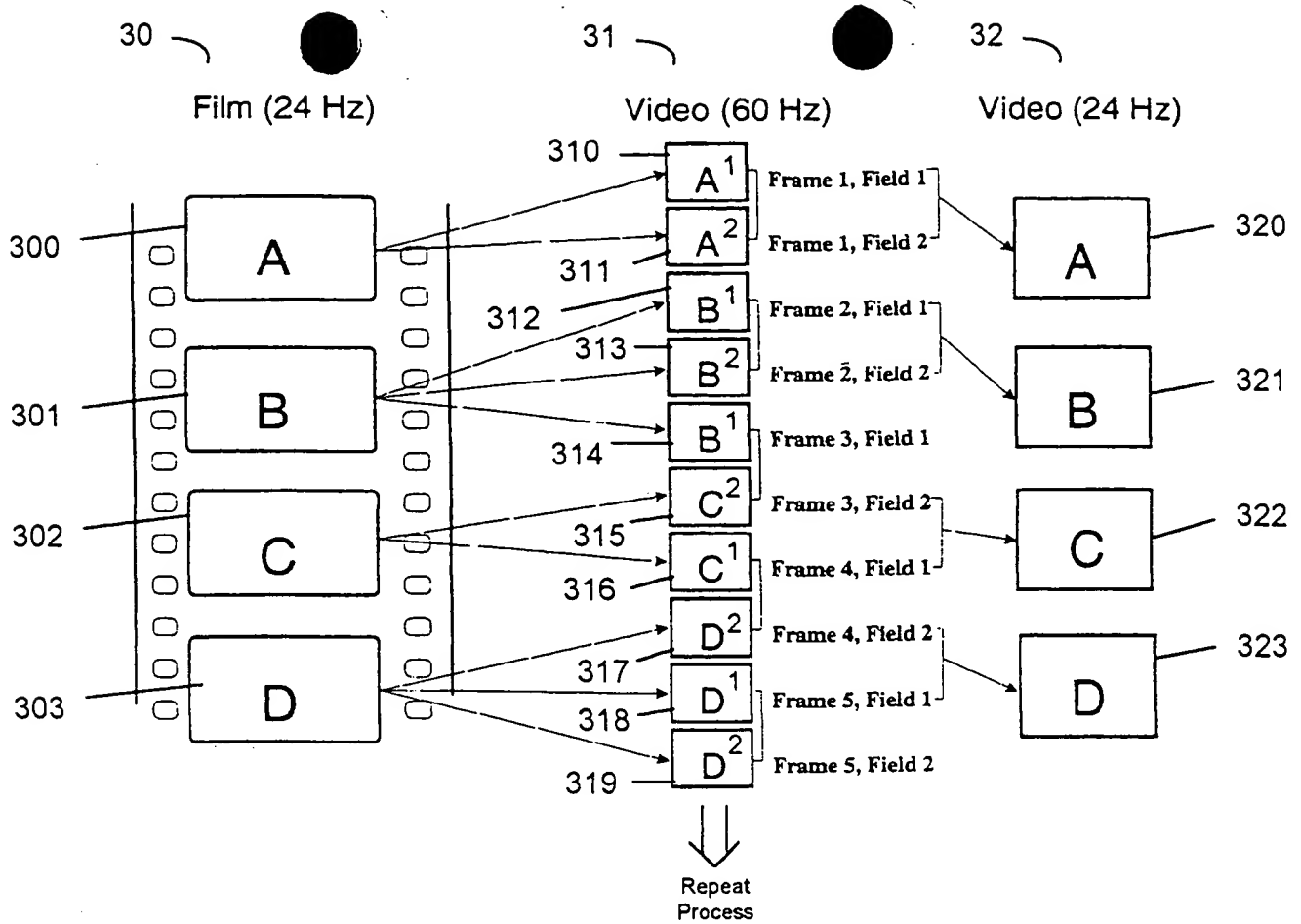


Fig. 3 (prior art)

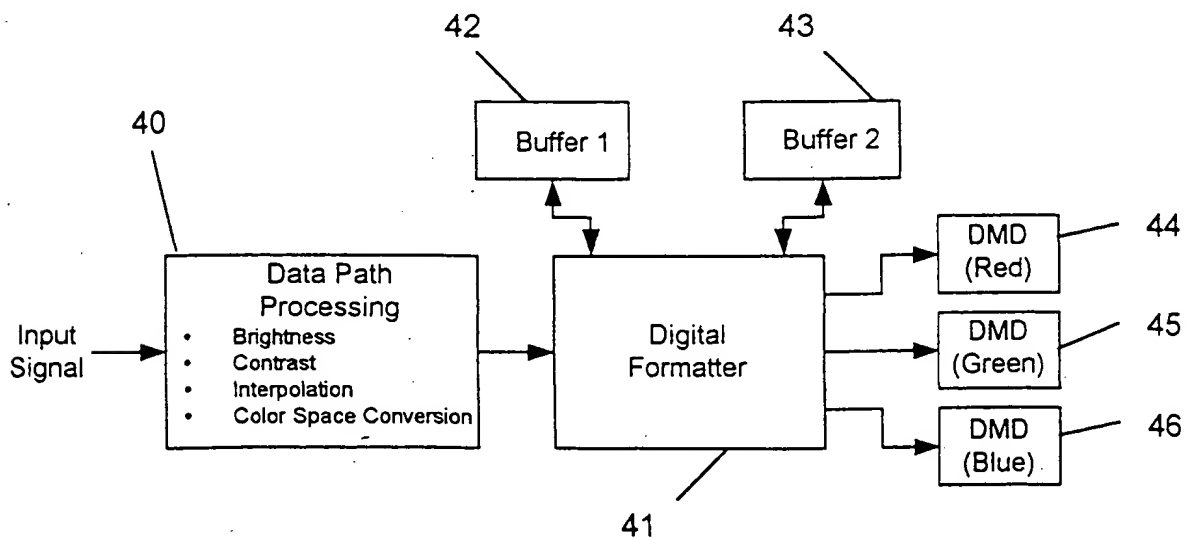


Fig. 4 (prior art)

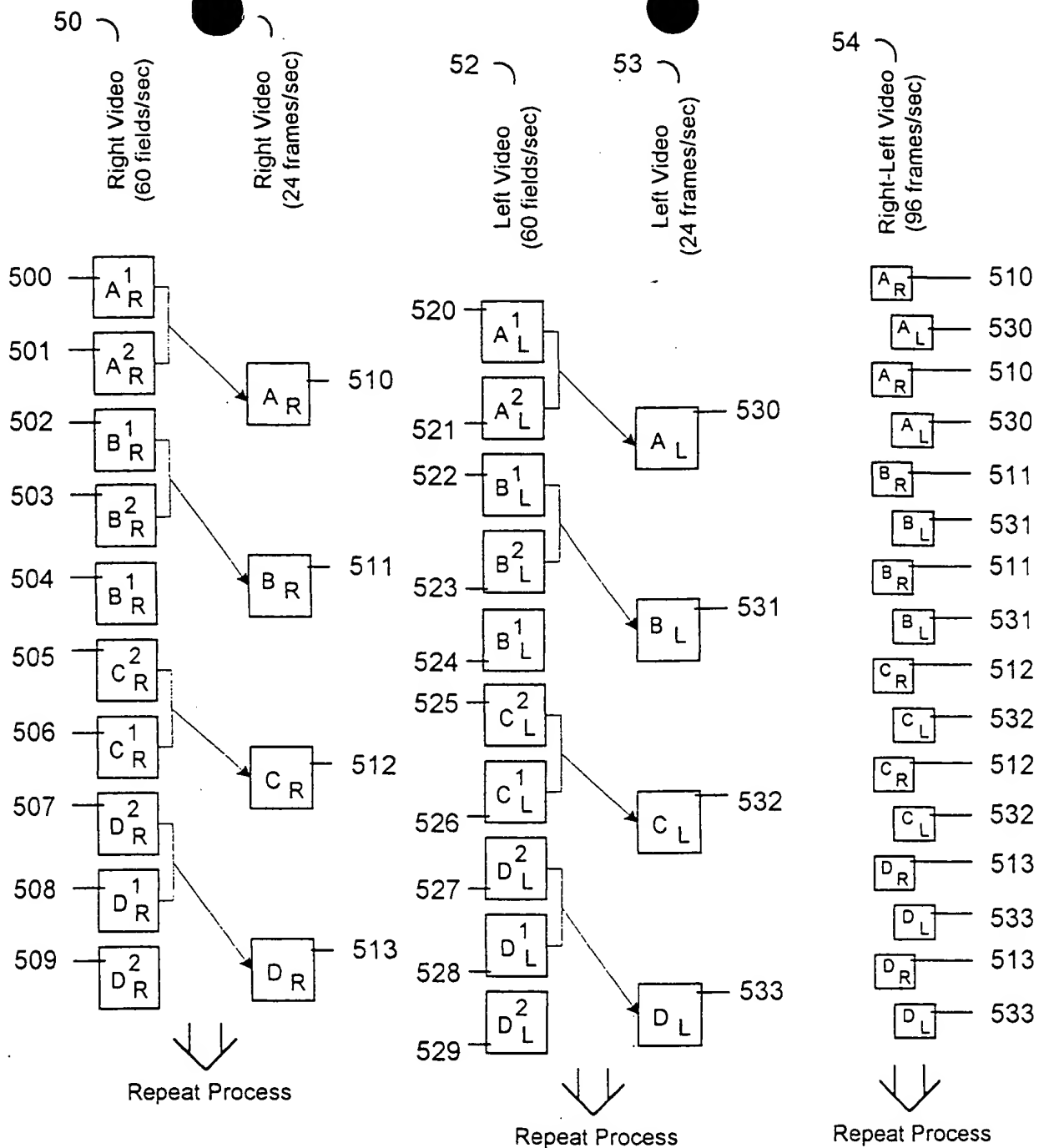


Fig. 5

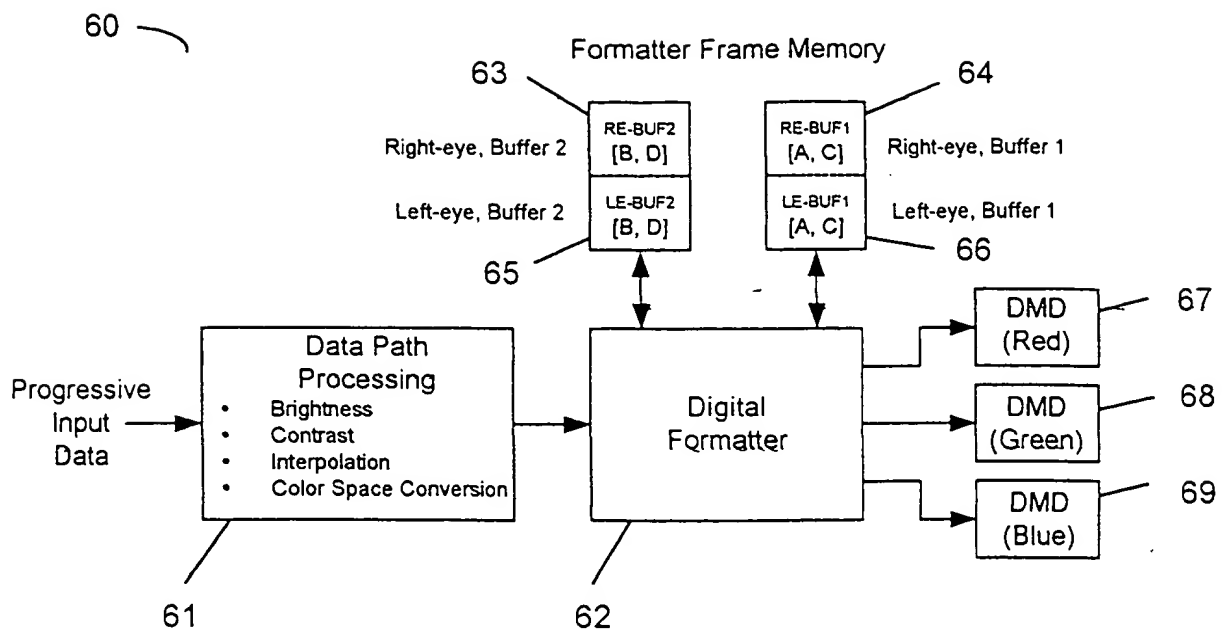


Fig. 6

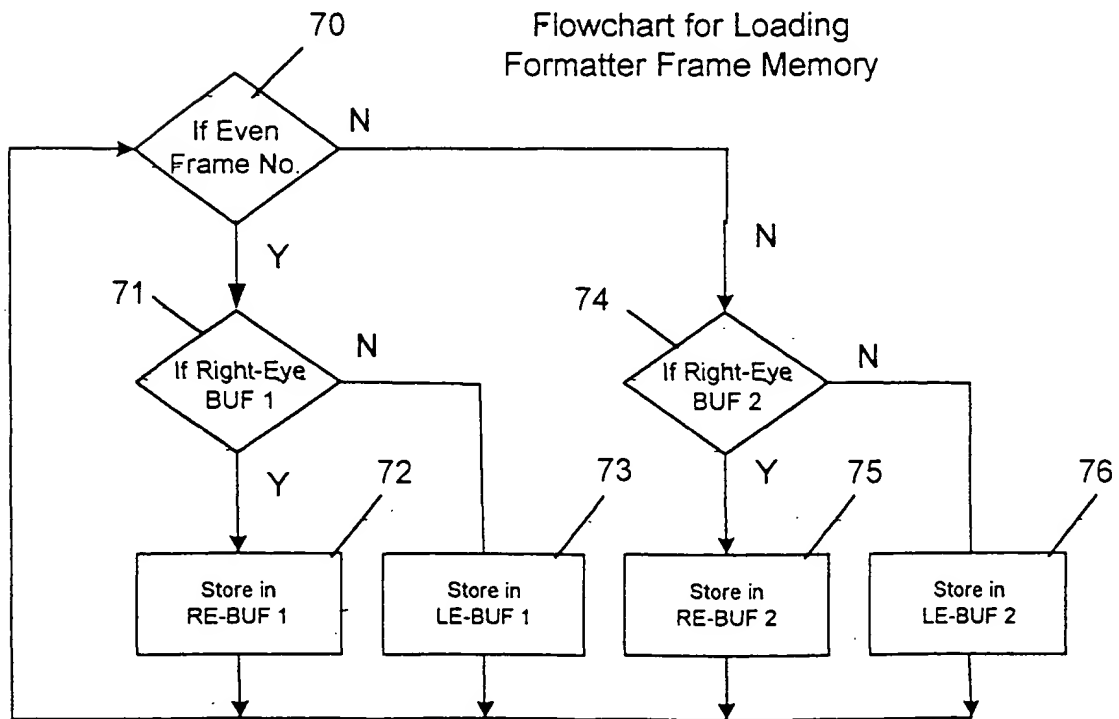


Fig. 7

Flowchart for
Displaying Data
from Formatter
Frame Memory

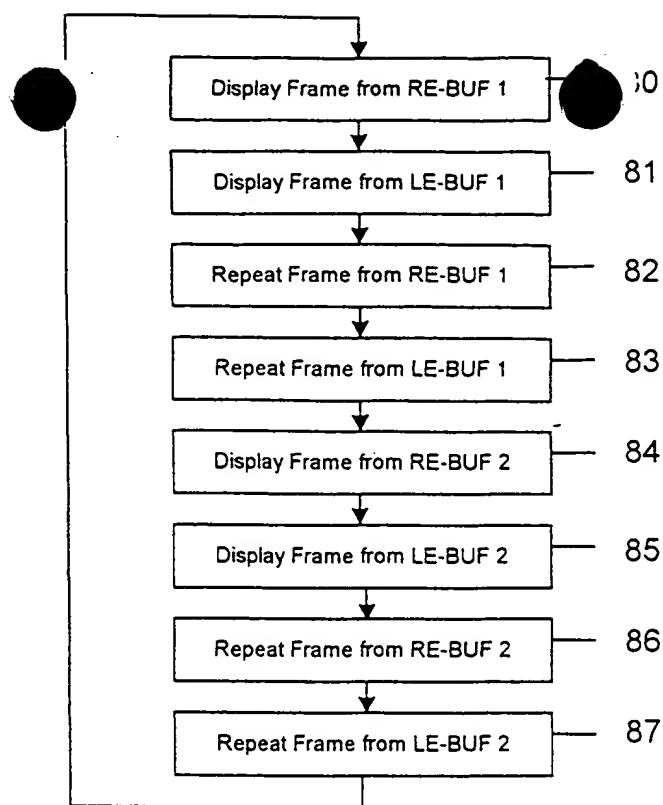


Fig. 8

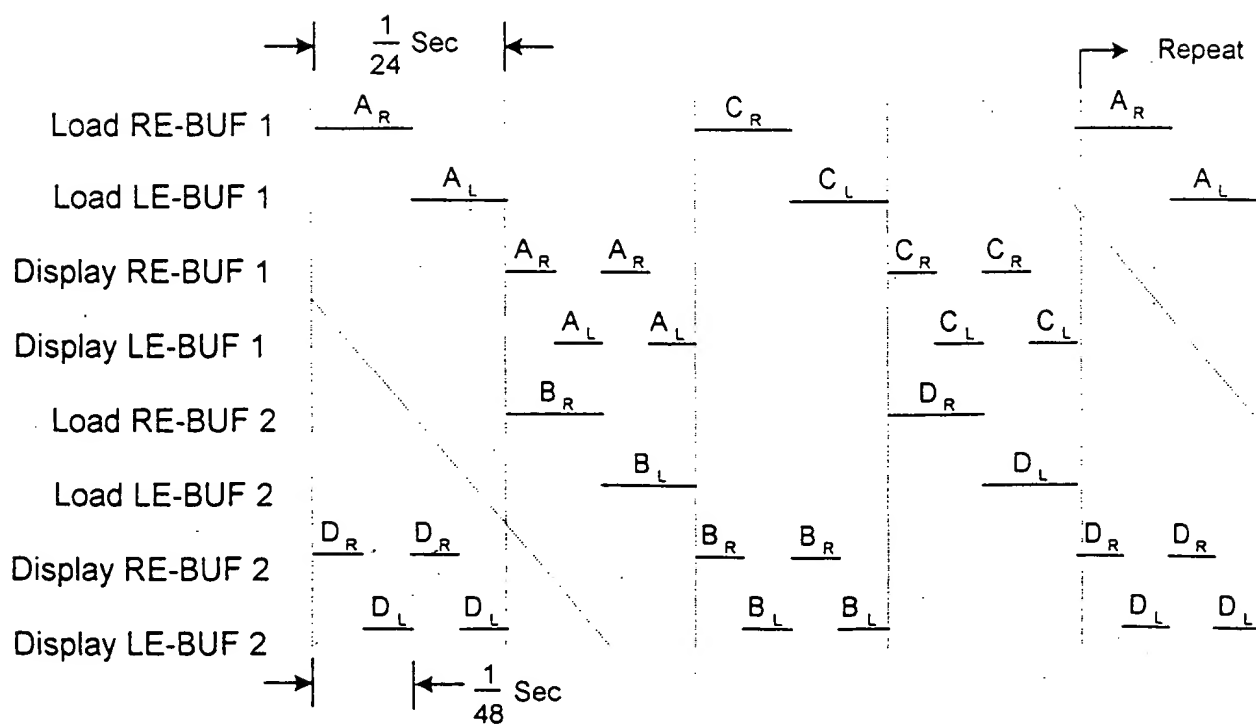
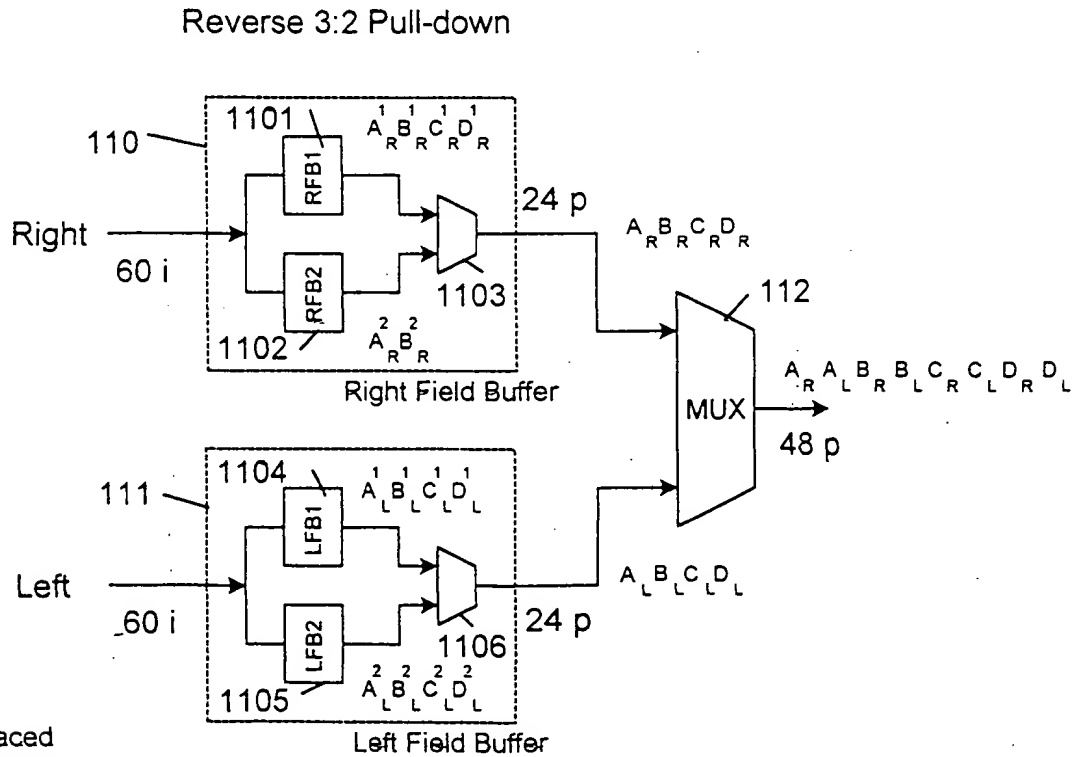
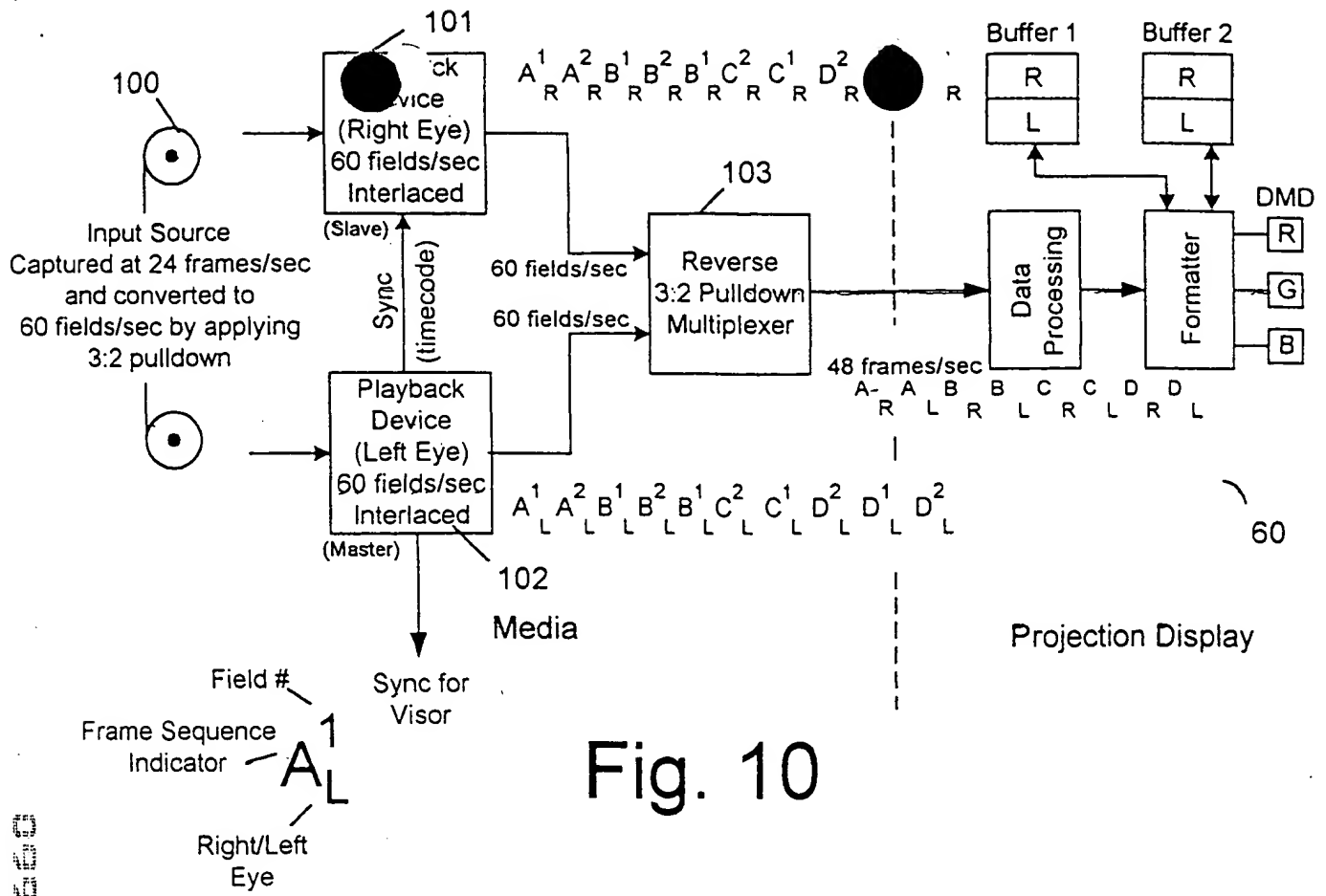


Fig. 9



60 i - 60 fields/sec, interlaced
24p - 24 frames/sec, progressive
48p - 48 frames/sec, progressive

Reverse 3:2 Pulldown Multiplexer - Input

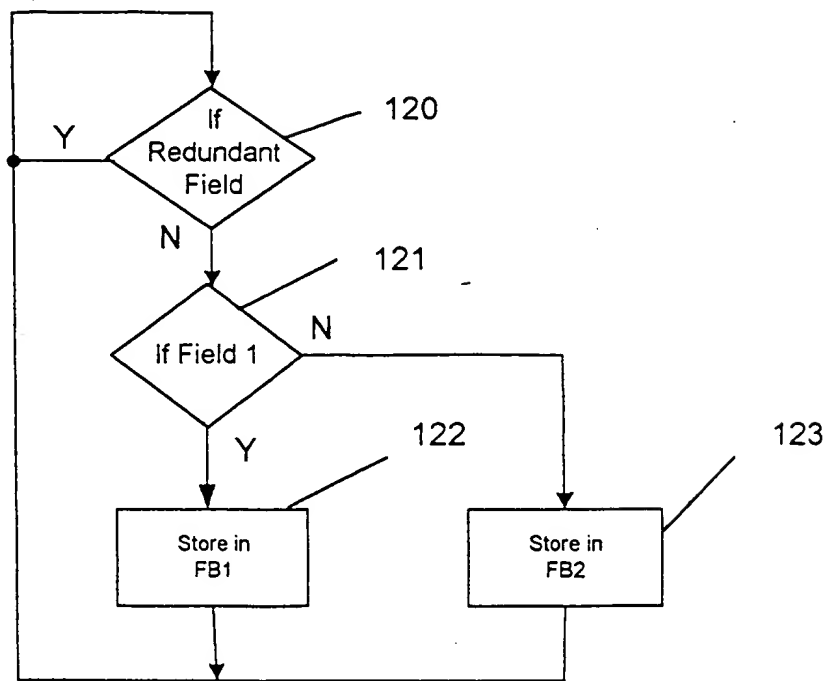


Fig. 12

Reverse 3:2 Pulldown Multiplexer - Output

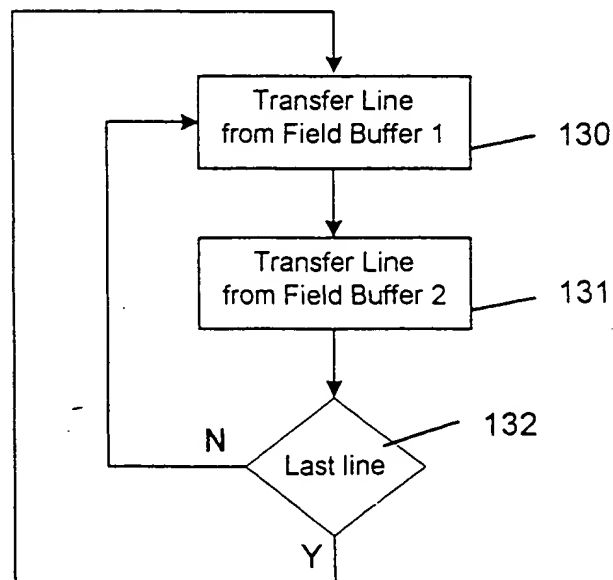
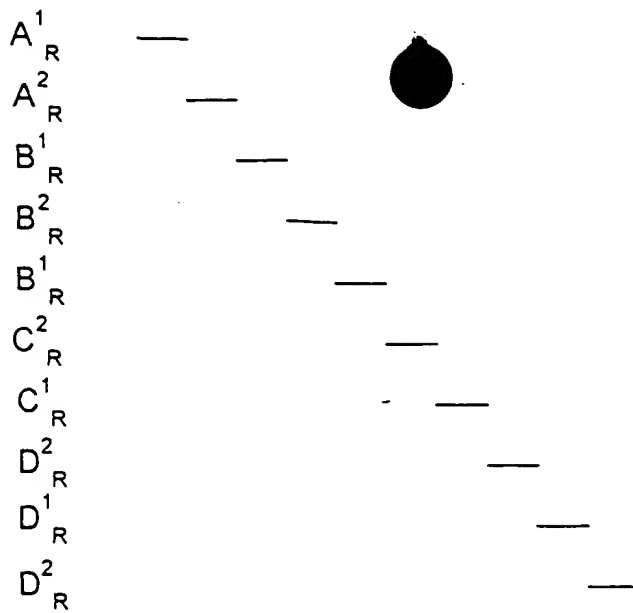
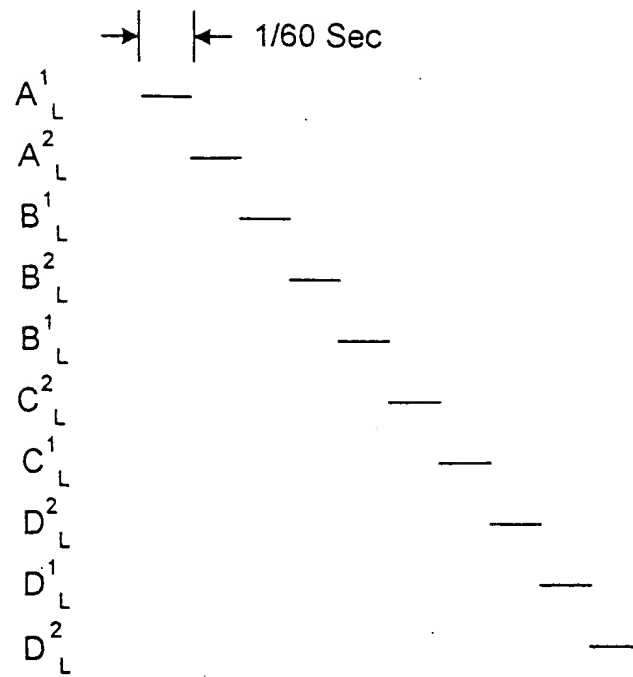


Fig. 13

Input to
Right Field
Buffer - 110



Input to
Left Field
Buffer - 111



Input to
MUX - 112

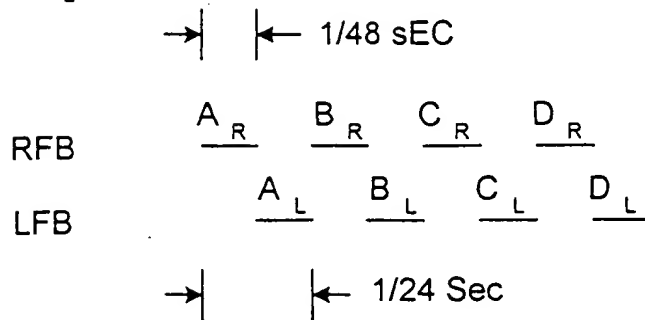


Fig. 14

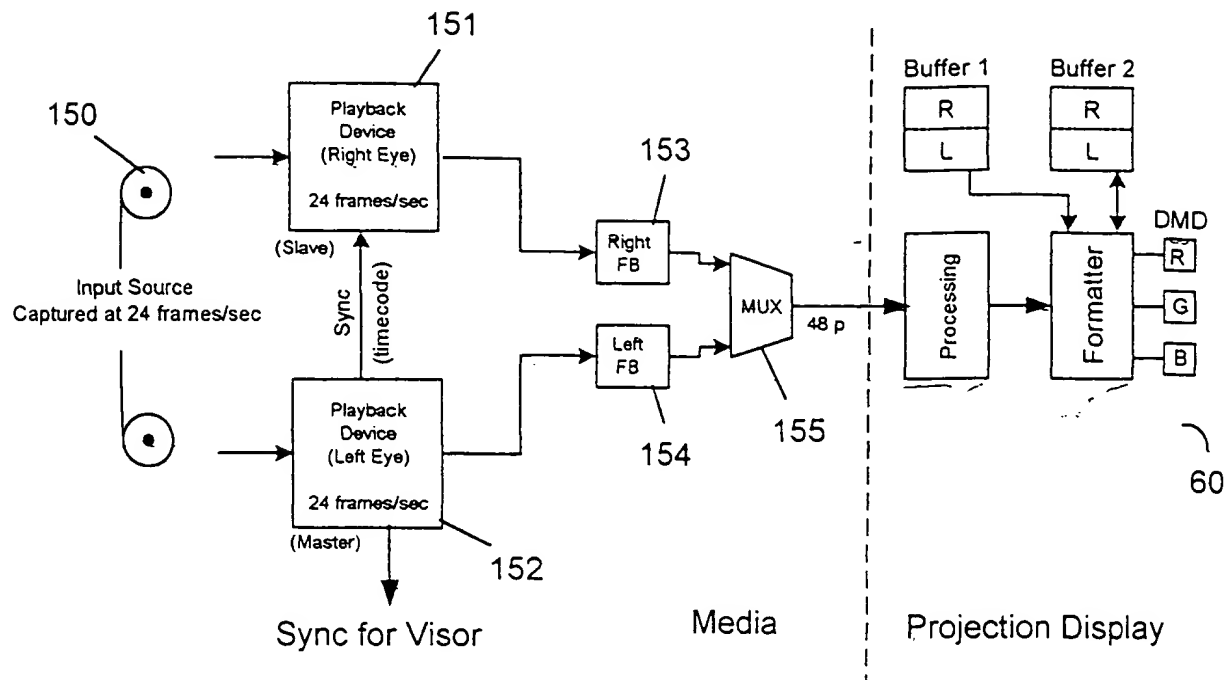


Fig. 15